AMENDMENTS TO THE CLAIMS

Please **AMEND** claims 14, 18, 19, and 20 as follows.

Please **CANCEL** claims 15-17 without prejudice or disclaimer.

Please **ADD** new claims 25 and 26 as follows.

A listing of all pending claims and the status identifiers appears below.

1-13 (canceled)

14. (currently amended) A circuit, comprising:

a lower semiconductor device comprising:

a first Si substrate;

a first SiO_2 layer formed on top of the first Si substrate; and

~~having an~~ a first active region comprising a semiconductor with a first crystal orientation formed on top of the first SiO_2 layer; ~~and~~

an upper semiconductor device comprising:

a second Si substrate;

a second SiO_2 layer formed atop the second Si substrate; and

~~having an~~ a second active region comprising a semiconductor with a second crystal orientation formed on top of the second SiO_2 layer~~,~~; and

a bonding layer disposed between a top of the lower semiconductor device and a bottom of the upper semiconductor device and bonding the upper semiconductor device to the lower semiconductor device,

wherein the upper semiconductor device is formed separately from the lower semiconductor device and connected thereto by an interconnect structure, and

the first crystal orientation is different from the second crystal orientation.

15. – 17. (canceled)

18. (currently amended) The circuit of claim 14, wherein ~~the upper semiconductor device is bonded to the top of the lower semiconductor device with an insulating layer, and wherein~~ at

least a portion of the upper semiconductor device is electrically connected to at least a portion of the lower semiconductor device.

19. (currently amended) The circuit of claim 18, wherein:

the lower semiconductor device includes ~~either~~ a pFET device ~~or an nFET device~~, and the upper semiconductor device includes ~~either a pFET device or~~ an nFET device~~; and~~

~~the crystal orientation of the active region of the respective lower semiconductor device is different from the crystal orientation of the active region of the respective upper semiconductor device~~.

20. (currently amended) The circuit of claim 18, wherein the lower and upper semiconductor devices comprise an inverter, and the pFET device has a crystal orientation of ~~[100]~~ [110] in an active region and the nFET device has a crystal orientation of ~~[110]~~ [100] in an active region.

21. (previously presented) The circuit of claim 18, further comprising a gate oxide formed on a top of the active region of the upper semiconductor device.

22. (previously presented) The circuit of claim 21, further comprising a poly gate formed on top of the gate oxide, with an upper poly contact to voltage bus.

23. (previously presented) The circuit of claim 22, further comprising metal contacts connecting to inputs of the upper semiconductor device.

24. (previously presented) The circuit of claim 23, further comprising a lower poly contact connecting to the voltage bus.

25. (new) The circuit of claim 18, wherein the lower semiconductor device includes an nFET device, and the upper semiconductor device includes a pFET device.

26. (new) The circuit of claim 25, wherein the lower and upper semiconductor devices comprise an inverter, and the pFET device has a crystal orientation of [110] in an active region and the nFET device has a crystal orientation of [100] in an active region.